Microprocessor & Interfacing
Lecture 27
8237 DMA Controller--2

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Registers

- Base Address
- Base Word Count
- Current Address
- Current Word Count
- Temporary Address
- Status
- Command
- Mode
- Mask Request

Registers

Name	Size	Number
Base Address Registers	16-bits	4
Base Word Count Registers	16-bits	4
Current Address Registers	16-bits	4
Current Word Count Registers	16-bits	4
Temporary Address Registers	16-bits	1
Temporary Word Count Registers	16-bits	1
Status Registers	8-bits	1
Command Registers	8-bits	1
Temporary Registers	8-bits	1
Mode Registers	6-bits	4
Mask Registers	4-bits	1
Request Registers	4-bits	1

Base Address Register

Each channel has 16 bit base address register

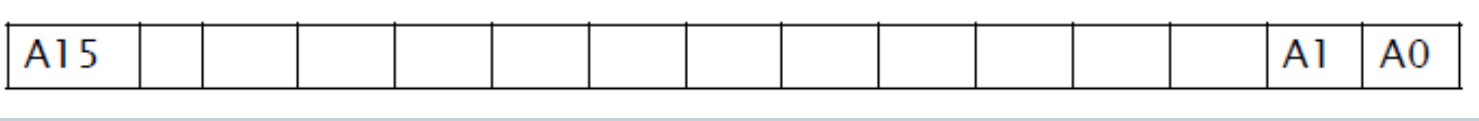
- It is a write only register
- It hold original value of address during all DMA transfer i.e. the content of this register not updated during DMA transfer
- When EOP' is activated the 8237 transfer content of base register into current address register in auto initialize mode.
- This register is written along with current address register during initialization format is same as current address register.

Base Word Count Register

- 16 bit, write only.
- It holds original count value during all DMA cycle means content of this register are not updated during DMA transfer.
- When EOP' is activated the 8237 transfer content of this register into current word register in autoinitialization mode.
- This register is written along with current address register during initialization format is same as current word register.

Current Address Register

- Each channel has 16 bit current address register,this register hold the address of memory location to be accessed during current DMA cycle.
- The address stored in this register is auto incremented or decremented after each transfer
- It is read and write register
- Divided into 2 parts lower byte & higher byte.
- In autoinitialization mode it initialized automatically with original address after EOP' signal



Current Word Count Register

- Each channel has 16 bit current word count register.
- The original value store in this register indicate the no of bytes to be transferred.
- The word count is decremented after each transfer the current count indicate the no of pending transfer.
- When the count value goes to zero a TC will be generated.
- It is a read and write register
- Divided into 2 parts lower byte & higher byte.
- In auto initialization mode it initialized automatically with original count value after EOP' signal the current word register format is
  - w15 w14 . .. .. w0

Temporary Address Register

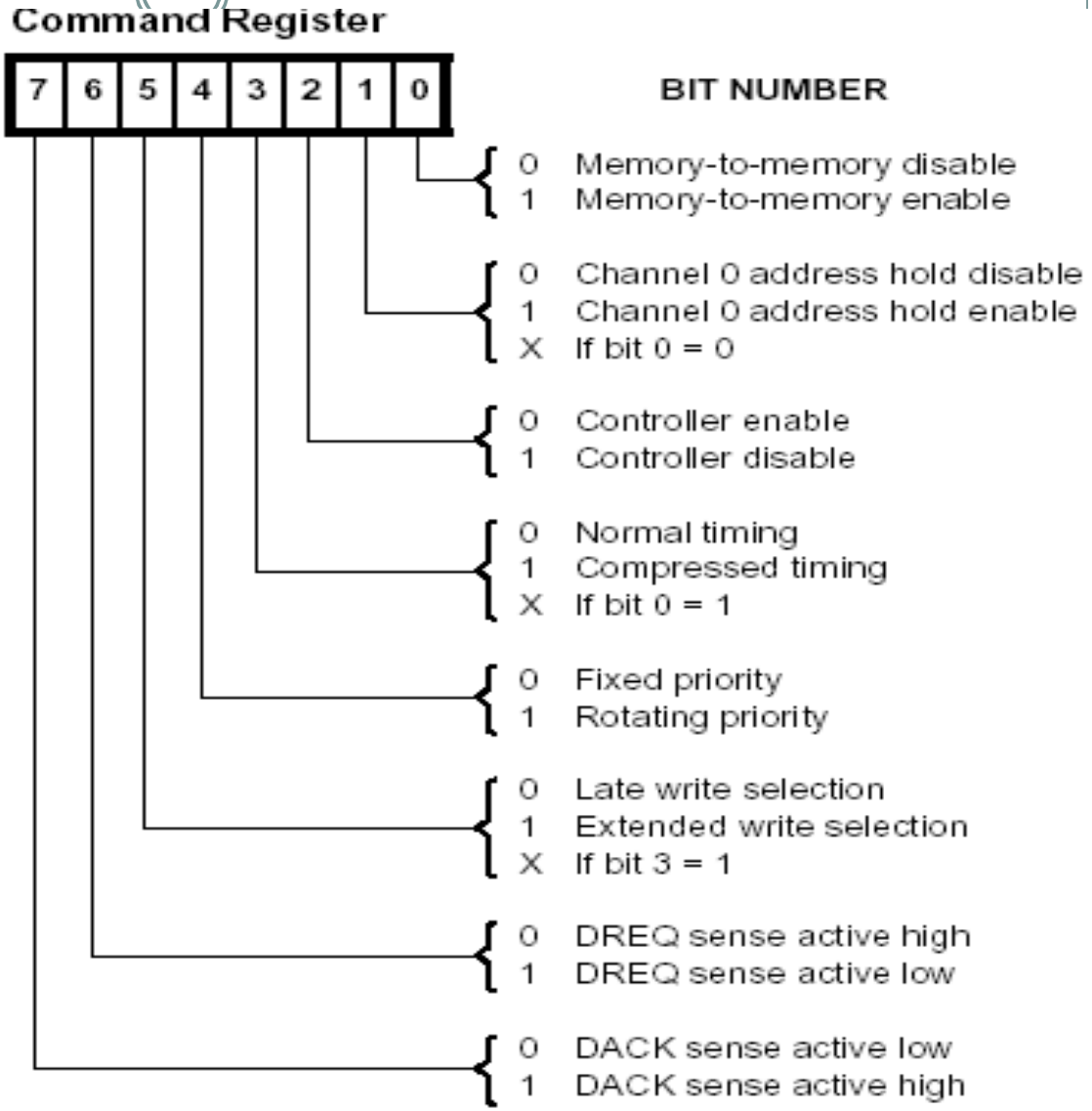
- This register is used to hold data during memory to memory transfer.
- It is 8 bit read only register.
- The microprocessor can read least byte of memory to memory transfer.
- It is cleared by reset signal.

Status Register

- 8-bit read only
- It indicate which channels have reached a terminal count and which channel has pending DMA.
- Bits 0-3 are every time a TC is reached by that channel or external EOP signal is applied.
- These bits are clear automatically on reading the status register and upon reset signal.
- Bits 4-7 are set whenever their corresponding channel is requesting service.
- D7 D6 ..... D1 D0
- Do if 0 channel reached TC if 1 not reach TC
- D1 if 1 channel reached TC if 1 not reach TC and so on

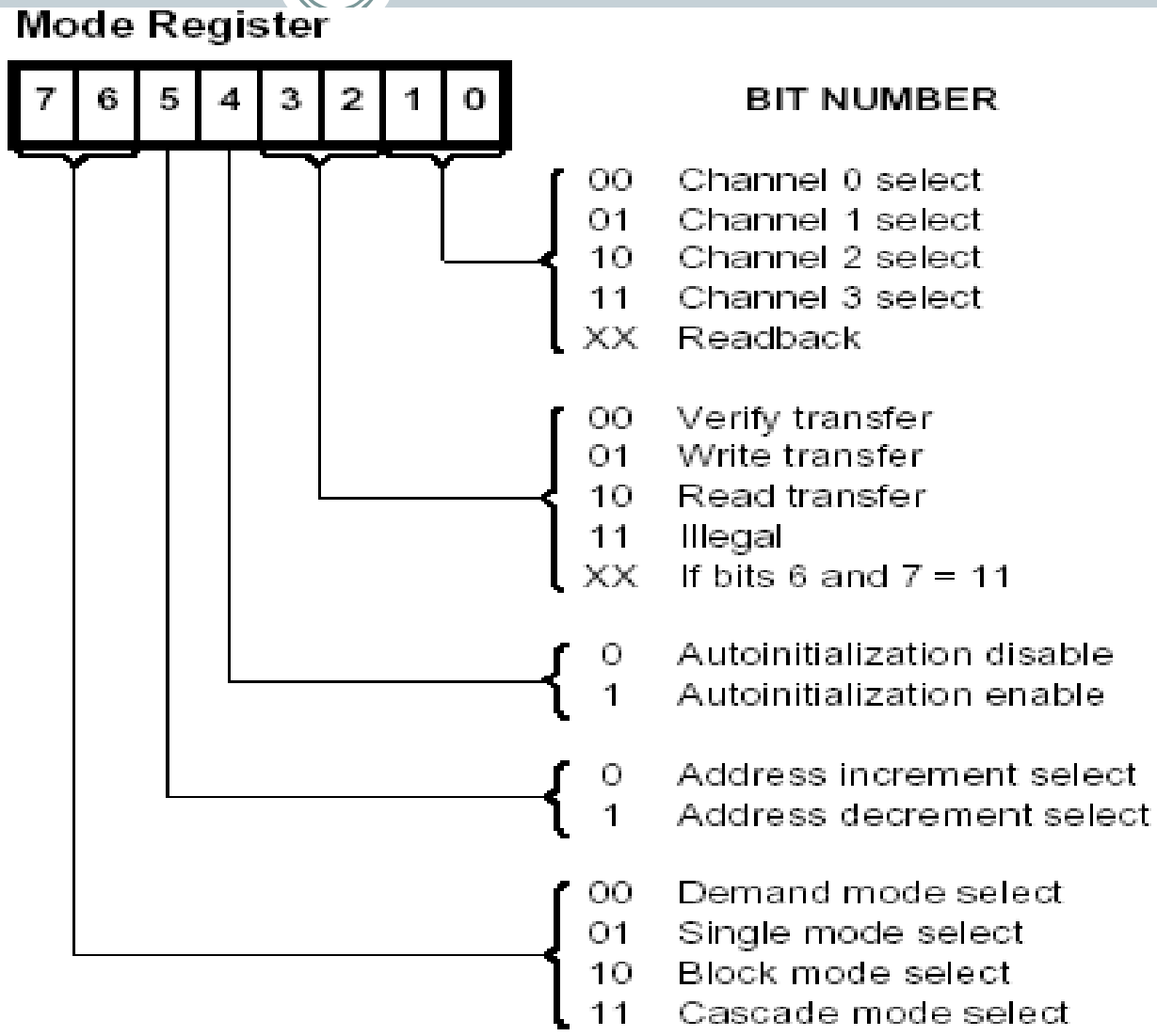
Command Register

- It is 8 bit write only register
- This register is cleared by reset signal
- It is used to initialize operational modes of 8237



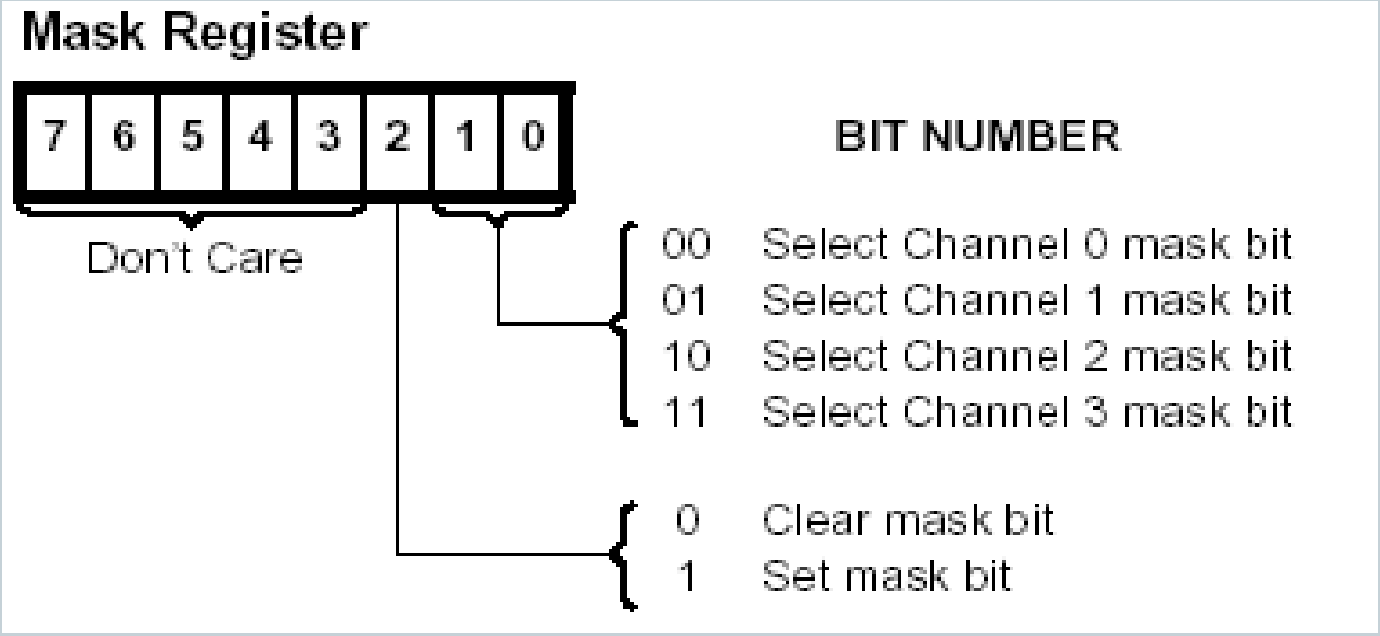
Mode Register

- It is 8bit write only register.
- It is used to set operative modes.
- Each channel has 6bit mode register.
- All register are clear by reset signal.



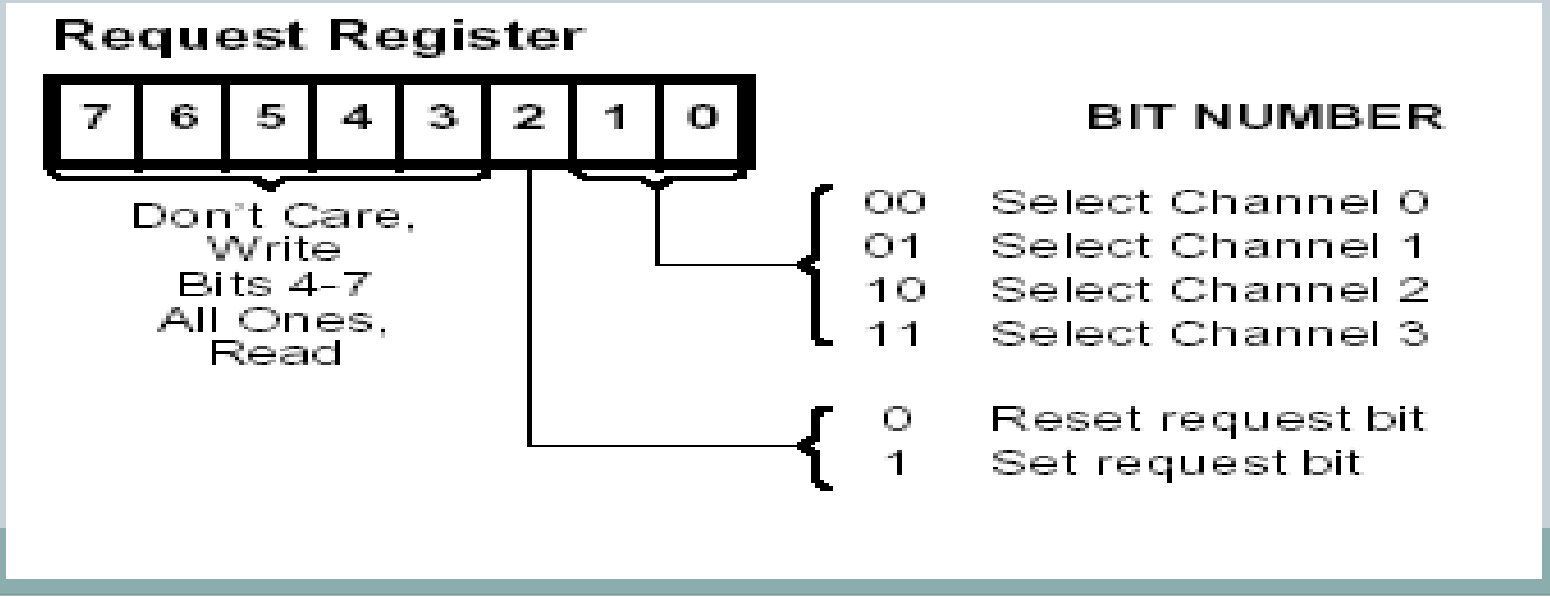
Mask Register

- It as a 8-bit write only register
- In normal mode mask bit set automatically after TC.
- It is not affected in autoinitialize mode



Request Register

- 8-bit write only
- It is used to request DMA through s/w. each channel has a request bit associated with in the request register.
- Each register is set or reset separately.
- Clear by reset



Block Transfer Mode

- In this mode device can make no of transfer as programmed in word count register.
- After each transfer count word is decremented by one and the address is decremented or incremented by one.
- The DMA transfer is untill the word count “roll over” from zero to FFFFh, a terminal count(TC) and external End of Process (EOP) is encountered. Block transfer mode is used when the DMAC needs to transfer a block of data.

Scope of Research

- DMA controller is widely used chip it transfer the data by passing the microprocessor. We can enhance the capability of DMA controller.